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Tuning Electrical and Optoelectronic Properties of Single Cadmium Telluride Nanoribbon

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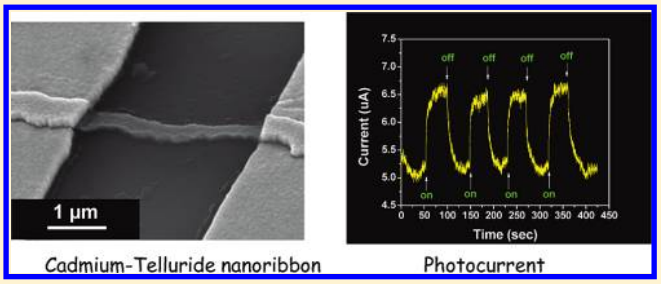
ABSTRACT: Cadmium telluride nanoribbons were synthesized electrochemically and formed into nanodevices using lithographically patterned nanowire electrodeposition (LPNE) that integrated synthesis and device fabrication together. By controlling the composition of the CdTe nanoribbons via adjusting the electrodeposition potential, electrical properties (i.e., electrical resistivity and field-effect transistor (FET) mobility) and optoelectronic property (photocurrent) were tuned and compared. Electrical resistivity of CdTe nanoribbons was strongly dependent on the Te content as higher Te content provided higher carrier concentration. Electrical conduction was limited by grain boundary traps due to polycrystalline structure. FET mobility was correlated to electrical resistivity and photocurrent, and annealed samples showed improved FET mobility, electrical resistivity, and photocurrent response.



INTRODUCTION

Cadmium Telluride (CdTe) is an important II−VI compound semiconductor because it has a direct band gap of 1.44 eV at room temperature with a high optical absorption coefficient[1] in the visible spectrum enabling it to be a great candidate material for photovoltaics. Indeed, CdTe thin film based solar cells have been investigated by many researchers[2−4] over the past decades and they are recently becoming commercially available. One-dimensional nanomaterials, such as nanowires, nanoribbons, and nanotubes, have been researched extensively because of their unique size dependent optical, electrical, and magnetic properties with potential application in nanoscale electronic, optoelectronic, spintronics, photovoltaics, thermoelectrics, and sensors.[5−14] Current research efforts have been focused on controlling the synthesis and integrating these nanoscale building blocks into high density complex devices. CdTe nanowires have been synthesized by a variety of techniques, including self-assembly from CdTe nanoparticles,[15] solution-based chemical synthesis,[16,17] and template-directed electrodeposition.[18−21] Although the synthesis of these CdTe nanowires have been demonstrated by various groups by a multitude of techniques, there exist very few reports on the electrical and optoelectronic properties of a single nanostructure based device. We have previously reported electrical and optoelectronic properties of a single CdTe nanowire for the first time.[21] We were able to synthesize CdTe nanowires with controlled composition and dimension using template directed electrodeposition; however, the fabrication yield of nanodevices with good electrical contact were very low, limiting our ability to investigate systematically the size and composition dependent electrical and optoelectronic properties.

A novel nanofabrication technique with a significant improvement over existing template-directed electrodeposition followed by device assembly known as lithographically patterned nanowire electrodeposition (LPNE) has been developed by the Penner group.[22−24] It retains many advantages of template-directed electrodeposition with a few improvements. One important advance of this technique is that it integrates both the bottom-up electrochemical synthesis of the nanomaterials and the top-down photolithography to fabricate batches of high density nanodevices with desired size and composition along with integrated microelectrodes. Typical nanodevice fabrication involves a batch synthesis of these nanowires followed by the assembly of the nanowires into nanodevices on a substrate using techniques such as e-beam lithography, focus ion beam (FIB), AC dielectrophoretic, and magnetic assembly, which are low-yield and costly. Another advantage of LPNE is that it allows precise location and orientation of the nanodevices on a wafer level improving the yields of functional devices, which is extremely attractive for mass production. Our group has also implemented this technique to fabricate Bi_2Te_3 and polypyrrole nanoribbon electrical nanodevices for thermoelectric and gas sensing applications.[13,14]

Single CdTe nanoribbon based devices were fabricated using LPNE technique, and their electrical and optoelectronic properties were shown to be tunable by the composition of the CdTe nanoribbons. Electrodeposition potential dictated the

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composition of the nanoribbons, which affected the electrical properties including electrical resistivity and FET mobility. Photocurrent was also shown to be directly affected by FET mobility demonstrating that higher photocurrent is achievable using CdTe nanoribbons with higher FET mobility.

EXPERIMENTAL MATERIALS AND METHODS

LPNE technique was used to synthesize CdTe nanoribbons with a slight protocol modification following other works from our research group.[13,14] Essentially, a sacrificial material, typically 100 or 25 nm of nickel, was e-beam evaporated on top of a p-type silicon wafer with a 300 nm silicon dioxide insulating layer. A layer of adhesion promoter Primer P20 (ShinEtsuMicroSi Microelectronic Materials) and photoresist S1813 (Rohm and HAAS Electronic Material) were spin coated on the sacrificial layer at 1000 rpm for 2 s followed by 4000 rpm for 30 s. The wafer was soft baked on a hot plate at 110 °C for 5 min. It was then exposed under UV lamp with a photomask to pattern the location of the nanoribbons and developed with diluted MF351 (Rohm and HAAS Electronic Material) in 1:5 ratio. Exposed nickel was chemically etched with a commercially available Nickel Etchant TFB (Transcene Company, Inc.) and followed by electrochemical etching to create an undercut beneath the photoresist. The electrochemically etching solutions contained 0.1 M potassium chloride and 24 mM hydrochloric acid. The etching potential and time was fixed at 0.02 V vs SCE and 5 min, respectively.

CdTe nanoribbons were then electrodeposited underneath the undercut at various deposition potential with a bath containing 1 M $CdSO_4$ + 0.30 mM TeO_2. The pH of solution was fixed at 2 with NaOH and/or H_2SO_4. After electrodeposition, photoresist was dissolved with acetone. Another layer of photoresist was spin coated with the same protocol followed by exposure to define the electrode patterns. It was developed, and chromium (20 nm) and gold (180 nm) were e-beam evaporated forming the electrode pads. The wafer was soaked in acetone for the final lift-off process. Lastly, the nickel was etched with 2% nitric acid. Some devices were annealed at 200 °C for 6 h under reducing environment (95% N_2 and 5% H_2).

The composition of the CdTe nanoribbons was determined by energy dispersive X-ray spectroscopy (EDAX). Scanning electron microscopy (SEM, Philips XL30 FEG) of CdTe nanoribbons was taken to determine the width and morphology of the nanoribbons. Electrical resistivity, FET properties, and photocurrent were measured with a Hewlett-Packard 4155A Semiconductor Parameter Analyzer at room temperature. Temperature dependent measurement was done under low pressure and darkness using a Keithley 236 Source Measure Unit interfaced with a CTI Cryodyne Refrigeration Systems and 8200 Compressor connected to a Lakeshore 331 Temperature Controller. For photocurrent measurement, a laser with a wavelength of 532 nm and an output power of 5mW was utilized as the light source.

RESULTS AND DISCUSSION

The electrical property of a CdTe nanoribbon can be tuned by controlling the dimensions, cross-sectional area, and length due to the relationship $R = \rho L/A$, where R is resistance, ρ is the electrical resistivity of the material, L is the length of the nanoribbons, and A is the cross-sectional area (thickness times width). LPNE allows for precise control over these parameters. The height of the nanoribbon was determined by the thickness of the sacrificial layer during the metal evaporation process with the e-beam evaporator. Nickel was chosen, mainly due to its relative ease of controlling etching rate both chemically and electrochemically, as the sacrificial layer with a thickness of 100 nm and 25 nm. The width of the CdTe nanoribbon was regulated by the duration of the electrodeposition. Figure 1

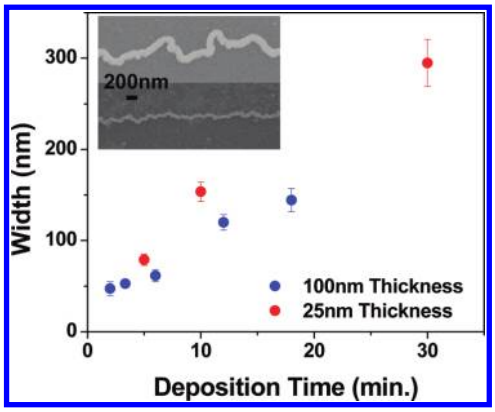

Figure 1. Width of CdTe nanoribbons as a function of deposition time. The inset shows SEM of nanoribbons.

shows a strong linear relationship between the width of the nanoribbons and the duration of the electrodeposition. LPNE technique was able to synthesize a continuous CdTe nanoribbon as narrow as ~40 nm wide. Length of the nanoribbon was dictated by the distance between the metal evaporated electrodes, which is limited by the resolution of the photolithography. In our experiment, the length of nanoribbons was varied from 3, 5, to 10 μm with different electrode patterns.

In addition to the dimensions of the nanoribbons, the electrical properties of nanoribbons are strongly dependent on the composition of nanoribbons, and the composition is controlled by deposition potential. Varying the deposition potential vs saturated calomel electrode (SCE) gave a wide range of compositions, from Te-rich to Cd-rich CdTe nanoribbons (Figure 2A). Near stoichiometric CdTe nanoribbons were electrodeposited at deposition potential of −0.65 V vs SCE. Deposition potential more negative than V = −0.70 V gave Cd-rich CdTe nanoribbons, whereas deposition potential more positive than V = −0.60 V gave Te-rich CdTe nanoribbons. The formation of Te-rich CdTe nanoribbons was due to the higher deposition rate of overpotential deposition of Te comparing to the relatively slower underpotential deposition of Cd^{2+} onto Te to form CdTe nanoribbons. When the deposition rates were equal, stoichiometric CdTe nanoribbons were deposited. To deposit Cd-rich CdTe nanoribbons, an overpotential deposition of Cd^{2+} was applied; however, the morphology of Cd-rich CdTe nanoribbons was ununiform and dendritic, which prevented devices to be fabricated for measurements. Electrical measurements presented in this work are of Te-rich down CdTe nanoribbons. These results are consistent with our previous result where the nanowires were synthesized via the template directed electrodeposition using ion track polycarbonate membrane as the scaffold indicating that the composition is strongly dependent upon the deposition potential regardless of the shape of the template (porous template vs trench template). Further in depth discussion on the electrodeposition, material characterization, and crystal quality characterization of CdTe nanostruc-

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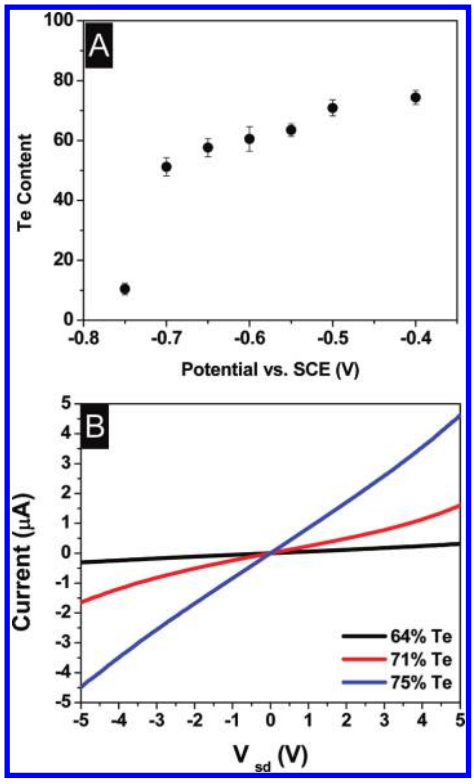

Figure 2. Composition of CdTe nanoribbons as a function of electrodeposition potential and $I-V_{sd}$ characteristic as a function of composition. (A) CdTe nanoribbons with varying composition are electrodeposited by applying different potential vs saturated calomel reference electrode. (B) Comparison of 3 CdTe nanoribbons at 64%, 71%, and 75% Te content with μ_{FET} at 0.07, 0.06, and 0.07 $cm^2/(V\ s)$, respectively.

ture fabricated via constant potential deposition has been presented in our previous work.[21]

The source-drain current versus source-drain voltage ($I_{sd}-V_{sd}$) characteristics of selected CdTe nanoribbons at 64% Te, 71% Te, and 75% Te composition with similar FET mobility (detail at the next section) at 0.07, 0.06, and 0.07 $cm^2/(V\ s)$ are compared (Figure 2B). Because mobility also affects resistivity, by selecting nanoribbons with similar mobility, the effect of % Te on resistivity becomes much clear and comparable. Devices show linear $I_{sd}-V_{sd}$ relationships indicating excellent ohmic contacts between the CdTe nanoribbons and the gold electrode pads. It is a significant improvement over our previous single CdTe nanowire based devices where the devices were fabricated by drop casting nanowires on top of electrode pads producing devices with Schottky barrier behavior because of a line contact between the nanowire and the electrode pads.[21] Calculated resistivities are 55.6 ohm cm (64% Te), 13.5 ohm cm (71% Te), and 5.3 ohm cm (74% Te) for these three CdTe nanoribbons. While FET mobility is kept constant, as the %Te content increases, the resistivity of the nanoribbons reduces indicating an increase in the carrier concentration. The relationship of increasing %Te resulting in decreasing resistivity is also consistent with our previous results.[21] In addition, this trend has been observed previously in p-CdTe electrodeposited thin films in which a similar inverse correlation between resistivity and deposition potential was correlated,[25,26] and a similar result on higher Te content giving lower resistivity of CdTe thin films was observed.[27]

The $I_{sd}-V_{sd}$ characteristics of a 64% Te-rich and a 75% Te-rich CdTe device are evaluated with gate voltage (V_g) set at $V_g = 0$, $V_g = -40$ V, and $V_g = 40$ V (Figure 3A). When a V_g of −40

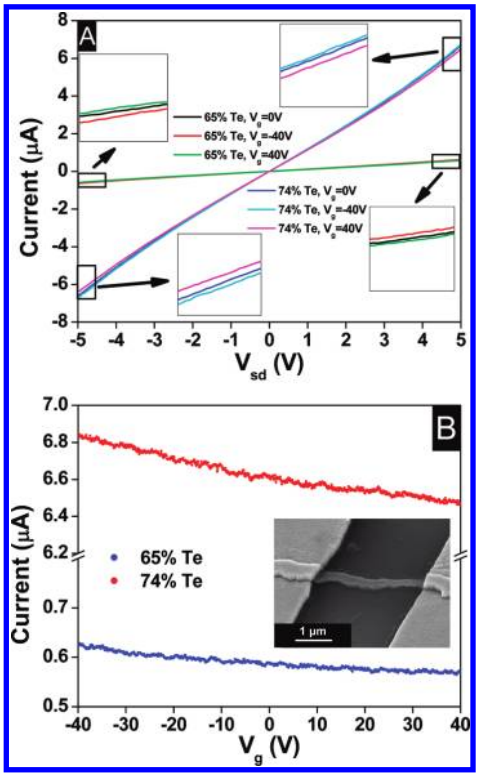

Figure 3. Current−source drain voltage ($I-V_{sd}$) and current−gate voltage ($I-V_g$) characteristics of a 65% Te and 74% Te CdTe nanoribbon with μ_{FET} at 0.22 and 0.23 $cm^2/(V\ s)$, respectively. (A) $I-V_{sd}$ of CdTe nanoribbons at $V_g = 0$ V, $V_g = -40$ V, and $V_g = 40$ V. (B) $I-V_g$ CdTe nanoribbons at $V_{sd} = 5$ V.

V was applied, the resistance decreased, while the resistance increased when V_g of 40 V was applied, indicating a field effect transistor (FET) behavior. This was also confirmed by the $I_{sd}-V_g$ characteristics of both devices with fixed V_{sd} at 5 V (Figure 3B). Both figures indicate that the Te-rich CdTe nanoribbons exhibit a p-type semiconductor behavior. When applying a more negative gate potential to a p-type semiconductor, accumulation of carriers leads to an increase of carrier concentration and conductance. In contrast, applying a more positive gate potential to a p-type semiconductor depletes carriers leading to a decrease of carrier concentration and conductance. The FET mobility, μ_{FET}, was determined from the transconductance ($g_m = \partial I_{sd}/\partial V_g$)[28,29]

$$\mu_{FET} = \frac{\partial I_{sd}}{\partial V_g}\frac{L^2}{V_{sd}C} \quad (1)$$

where the gate capacitance $C = \varepsilon\varepsilon_0 A/d$ assuming a parallel plate model for a nanoribbon geometry, ε is the dielectric constant of SiO_2, ε_0 is the permittivity, A is the cross-sectional area of the nanoribbon, and d is the thickness of the SiO_2 dielectric layer. For these two CdTe nanoribbons (Figure 3B), μ_{FET} is determined to be 0.22 and 0.23 $cm^2/(V\ s)$ at $V_{sd} = 5$ V. Our calculated μ_{FET}, ranging from 0.01 to 2 $cm^2/(V\ s)$ for various Te-rich p-type CdTe composition, is comparable to hole mobility that was measured using Hall measurement technique on electrodeposited CdTe thin film devices with a value of 1

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$cm^2/(V\ s)$.[26] Single crystal bulk CdTe has been reported to have a much higher hole mobility of 80 $cm^2/(V\ s)$ for p-type and 1050 $cm^2/(V\ s)$ for n-type CdTe.[25] Our values are 2 orders of magnitude lower than the single crystal stoichiometric bulk CdTe, but they are similar to electrodeposited CdTe thin film. The difference is due to the electron scattering and carrier trappings at the grain boundaries of a polycrystalline structure, and it has been shown that the mobility of CdTe thin film was strongly affected by the grain boundary scattering for a polycrystalline CdTe film.[25] In comparison with other II−VI semiconductor materials, cadmium selenide (CdSe) in thin film transistors configuration has been reported to have a μ_{FET} value of 1−7 $cm^2/(V\ s)$[30] and 5−15 $cm^2/(V\ s)$,[31] whereas n-type cadmium sulfide (CdS) thin film transistors has been reported to be 0.2−1 $cm^2/(V\ s)$.[31] A slightly higher μ_{FET} value of 9.6 $cm^2/(V\ s)$ was obtained for a single crystal n-type CdSe nanoribbon fabricated by thermal evaporation method.[32] Interestingly, an n-type CdS nanoribbon has been demonstrated to have a high μ_{FET} value of 283 $cm^2/(V\ s)$,[33] which matches very closely to the single crystal n-type CdS bulk mobility value of 300−350 $cm^2/(V\ s)$. Again, the high carrier mobility was attributed to the excellent crystalline quality of the CdS nanoribbon.

The grain boundary trapping model, developed by Seto[34] and later improved by Baccarani,[35] explained how grain boundary limits the conduction for a polycrystalline material. Because of the grain boundary having dangling bonds, there are trapping states at the grain boundary able to capture and immobilize carriers resulting in a reduction of the available carriers. Once they become trapped, they are electrically charged becoming potential barriers consequently reducing carrier mobility. Current across the grain boundary is a contribution of thermionic emission, carriers having enough energy to go over the barrier, and tunneling, carriers going through the barrier via quantum mechanical tunneling. The potential barrier height is estimated by $\sigma \propto \exp(-E_b/kT)$ where σ is conductivity, E_b is the barrier height, k is the Boltzmann constant, and T is temperature. The barrier height, due to traps at grain boundary, calculated from the slope near the room temperature region is 72 meV (Figure 4). At low temperature, current is dominated by the tunneling mechanism as conduction becomes less temperature sensitive. Lastly, having a characteristic of negative temperature coefficient of resistance, resistance decreases as temperature increases, shows that the CdTe nanoribbon behaves as a typical semiconductor.

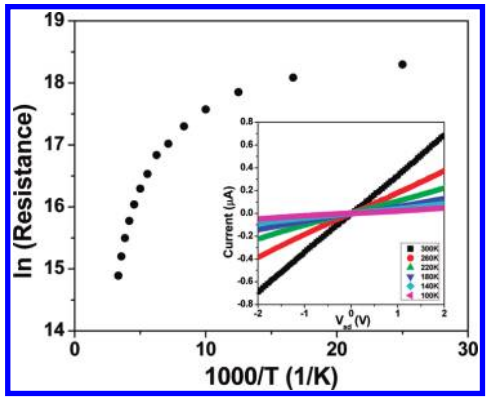

Figure 4. Temperature dependency of resistance. The inset shows I_{sd}−V_{sd} characteristics at various selected temperature.

To demonstrate that FET mobility is affected by the crystalline quality of the CdTe nanoribbons, CdTe nanoribbons were annealed at 200 °C for 6 h, and their I_{sd}−V_{sd} and I_{sd}−V_g characteristics were measured to highlight the effect of grain growth from the annealing process (Figure 5A,B). In this

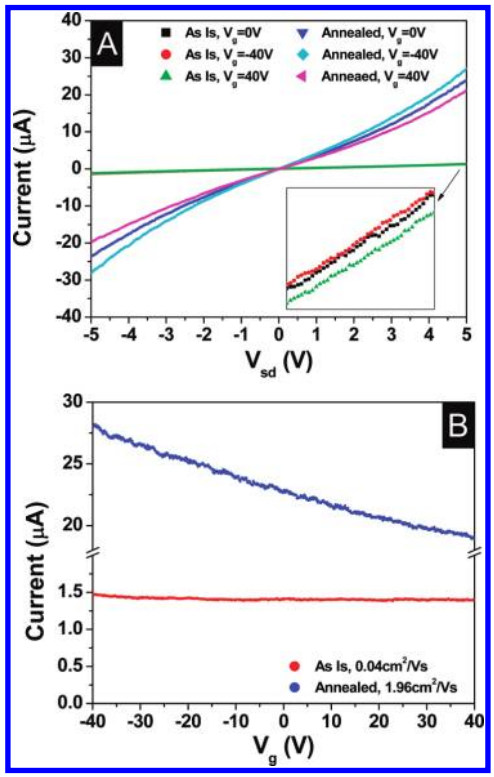

Figure 5. Effect of annealing to current−source drain voltage (I−V_{sd}) and current−gate voltage (I−V_g) characteristics of CdTe nanoribbons. (A) I−V_{sd} of CdTe nanoribbons at V_g = 0 V, V_g = −40 V, and V_g = 40 V before and after annealing. (B) I−V_g of CdTe nanoribbons at V_{sd} = 5 V before and after annealing.

example, μ_{FET} has increased from 0.04 to 1.96 $cm^2/(V\ s)$, and resistivity has reduced from 43 to 3 ohm cm. This improvement of μ_{FET} is due to a reduction of scattering at the grain boundaries as the grain size grows during the annealing process. From a sample size of 11 CdTe nanoribbons, typical increase in μ_{FET} ranges from 8- to 80-fold after the annealing process (data not shown). At the same time, the resistivity has not reduced proportionally as μ_{FET} has increased indicating that the carrier concentration has been affected by the annealing process as well. Data suggests that the carrier concentration has been reduced by an average of 3-fold by the annealing process. To summarize the relationship between FET mobility and resistivity, they were plotted showing an inverse correlation (Figure 6). The scattering of the data is a result of nanoribbons having varying carrier concentration. In summary, Figures 1−6 demonstrate that the electrical characteristics can be modified (1) by manipulating the dimension of the nanoribbons via the adjustment of parameters (sacrificial layer thickness, deposition time, and distance between contacts), (2) by varying the composition of the CdTe nanoribbon, which is adjusted by the electrodeposition potential to control the carrier concentration, and (3) by annealing to increase FET mobility through increasing grain size.

Figure 7A shows the change of the I_{sd}−V_{sd} characteristics and compares the photocurrent of 2 Te-rich p-CdTe nanoribbons,

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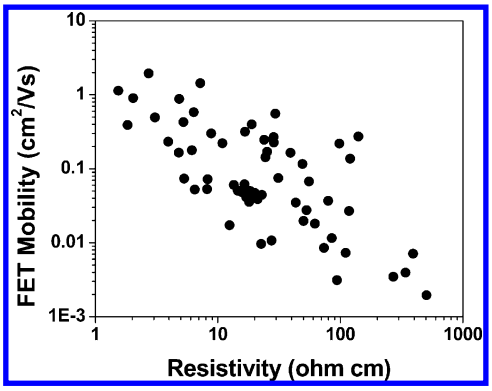

Figure 6. Correlations between composition, resistivity, and FET mobility of CdTe nanoribbons. FET mobility and resistivity are inversely correlated. As the resistivity of the CdTe nanoribbon increases, the FET mobility decreases.

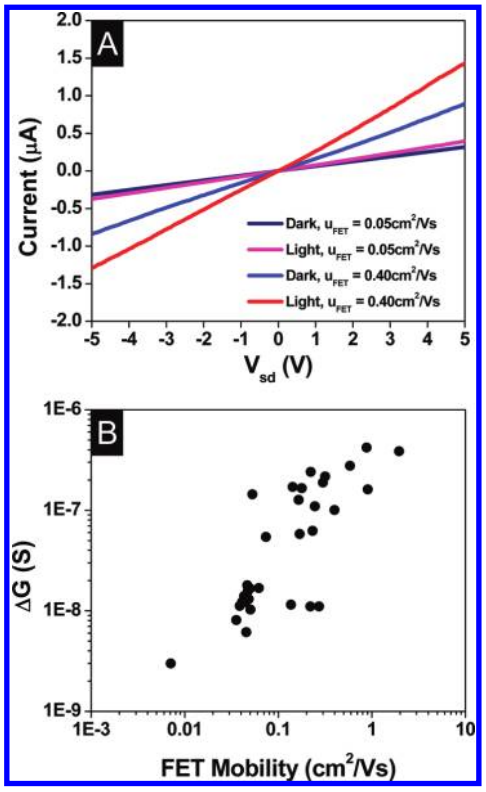

Figure 7. Effect of FET mobility to photocurrent. (A) Comparison of I vs V_{sd} under dark and light for CdTe nanoribbons with μ_{FET} at 0.048 $cm^2/(V\ s)$ and 0.398 $cm^2/(V\ s)$. (B) Photocurrent at V_{sd} = 1 V as a function of FET mobility.

μ_{FET} = 0.05 $cm^2/(V\ s)$, ρ = 15.7 ohm cm vs μ_{FET} = 0.40 $cm^2/(V\ s)$, ρ = 18.9 ohm cm, upon exposure to light illumination at λ = 532 nm. When the photon energy is greater than the band gap energy, it is absorbed by the electrons in the valence band and excited into the conduction band leaving hole carriers behind. These photogenerated electron–hole pairs contribute to an increase in carrier concentration and thus decrease the resistivity of the direct band gap material. Photoconductive gain of a nanoribbon by illumination can be defined as

$$G = \left(\frac{I_{ph}}{P}\right)\left(\frac{h\nu}{q}\right) = R\left(\frac{h\nu}{q}\right) = \frac{\mu\tau E}{L^2} \quad (2)$$

where P is the power absorbed in the nanoribbon, I_{ph} is the photocurrent, q is the elementary charge, $h\nu$ is the photon energy, R is the responsivity, μ is the carrier mobility, τ is the carrier lifetime, E is the electric field, and L is the length of the nanoribbon. A photoconductive gain of 1.13 and 12.2 was calculated at V_{sd} = 1 V for nanoribbons in Figure 7A, and even higher photoconductive gain could be obtained at higher V_{sd}. This photoconductive gain is consistent with LPNE fabricated CdSe nanowire arrays that has been reported to have G from 0.017 to 4.9 as grain size increases.[24] Single crystal n-type CdSe nanowire grown by the solution–liquid–solid technique has been reported to have a decrease of resistivity from 2- to 100-fold from different devices upon light exposure.[36] Compared to other single crystalline nanostructures (e.g., ZnO ($G = 2 \times 10^8$),[37] GaN ($G = 10^5$),[38] and Ge[39]), the cause of low photoconductive gain is attributed to the polycrystalline quality of CdTe nanoribbons, which contained many grain boundaries. Recombination of electron–hole pairs at the grain boundaries occurs readily and reduces the photocurrent of the device. By defining the change in conductance ΔG as $(I_{light} - I_{dark})/V_{sd}$, the change in photocurrent, in terms of conductance, was correlated to the FET mobility (Figure 7B). As the FET mobility of the devices increased, the photocurrent also increased, which supports eq 2, and that the low photocurrent was limited by the low mobility of the carriers of the device.

Time-resolved photocurrent measurement was acquired by turning on and off the light source during the current–time measurement for one device with a higher FET mobility (μ_{FET} = 0.32 $cm^2/(V\ s)$) and another device with a lower FET mobility (μ_{FET} < 0.01 $cm^2/(V\ s)$) obtained after both devices were annealed at 200 °C for 6 h (Figure 8). Both devices

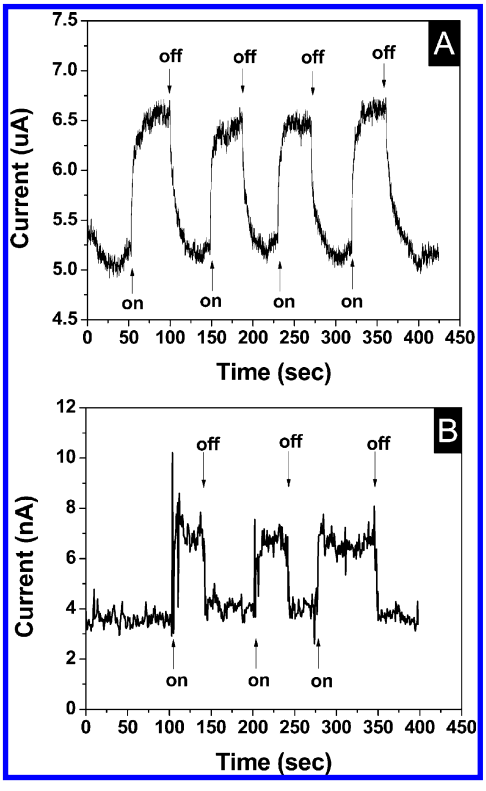

Figure 8. Time-resolved photocurrent measurement of (A) one device with μ_{FET} = 0.32 $cm^2/(V\ s)$ versus (B) another device with μ_{FET} < 0.01 $cm^2/(V\ s)$.

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responded accordingly as the light source was turned on and off. Higher mobility CdTe nanoribbons produced a higher photocurrent than the lower mobility CdTe nanoribbons. This portion is well understood according to eq 2 as I_{ph} is proportional to μ. The difference in the 3 orders of magnitude of I_{ph} (μA vs nA) is consistent since the difference of μ_{FET} between the devices was about 3 orders of magnitude. Since there is a direct correlation between grain size and mobility,[24] controlling grain size provides the means to control I_{ph}.

Mobility−lifetime product, $\mu\tau$, is an important figure of merit for charge collecting devices. Higher mobility and longer effective lifetime of carriers contribute to higher efficiency in collecting photogenerated charges; however, longer effective lifetime also contributes to longer response and decay times as there is a trade-off between speed and gain. Devices with a higher I_{ph} (Figure 8A) also clearly exhibited a response time and a decay time as the light source was turned on and off, while the device with a lower I_{ph} in Figure 8B responded much faster. Response time for the higher I_{ph} (μ_{FET} = 0.32 cm^2/(V s)) CdTe nanoribbons was estimated to be 11 ± 2 s, while the decay time was longer at 21 ± 8 s. For the lower I_{ph} (μ_{FET} < 0.01 cm^2/(V s)) CdTe nanoribbons, the response time was approximately 3.5 s ± 3 s with a decay time of 2.5 ± 1.5 s. The long response and decay time is associated with the trapping and untrapping rate being much slower than the rate of the carrier recombination process. Since photocurrent existed after the light source has been cut off for some time, the carriers must not be swept out of the device for a period of time. These nearly immobile holes, and not yet recombined, allow the photocurrent to remain after the light source has been cut off. Although the mechanism of the carrier lifetime of photosensitive devices has also been associated with the trapping of electron−hole pairs due to surface reaction,[37,39,40] such is not the case for our CdTe nanoribbons because the I_{sd}−V_{sd} characteristics remain similar under normal room conditions versus under low pressure. Another contribution to the difference in the carrier mobility−lifetime product of the devices is the trapping sites at the grain boundaries due to the difference in the grain size of the devices. This is the more likely scenario for these CdTe nanoribbons. The proportional correlation between I_{ph} and response/decay time as a result of increased of grain size has also been observed for LPNE fabricated CdSe nanowire arrays.[24]

CONCLUSIONS

Lithographically patterned nanowire electrodeposition technique was utilized to synthesize CdTe nanoribbons with controlled dimensions and composition, and their electrical and optoelectrical properties were systematically investigated. Varying composition of Te-rich CdTe nanoribbons were electrodeposited by controlling applied deposition potential, and electrical resistivity of nanoribbons was strongly depended on Te content. Temperature dependent resistivity measurement showed a negative temperature coefficient of resistance and that the electrical conduction was limited by potential barrier height due to grain boundary. By controlling the FET mobility of the CdTe nanoribbons via annealing, improved electrical and optoelectronic properties were obtained. I_{sd}−V_{sd} characteristics of photocurrent and time-resolved photocurrent measurement demonstrated and compared the effect of μ_{FET} to the photocurrent, and the effect of photocurrent to the response/decay time of the CdTe nanoribbon devices. LPNE offers a powerful tool to fine-tune the electrical property of nanostructures not only for CdTe but potentially for various compound semiconductor materials that can be electrodeposited. Further works that will be of interests are (1) modifying electrodeposition conditions to produce lithographically pattern-able Cd-rich CdTe nanoribbons for electrical and optoelectronic measurements, (2) correlation of grain size to varying electrodeposition conditions and mobility, (3) determining grain boundary trap density[34] from temperature dependent measurement and carrier concentration for various composition and grain size of nanoribbons, and (4) correlating trap density to various parameters of photocurrent.

AUTHOR INFORMATION

Notes

The authors declare no competing financial interest.

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